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(71) Applicant:
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
Kadoma-shi, Osaka 571-8501 (JP)

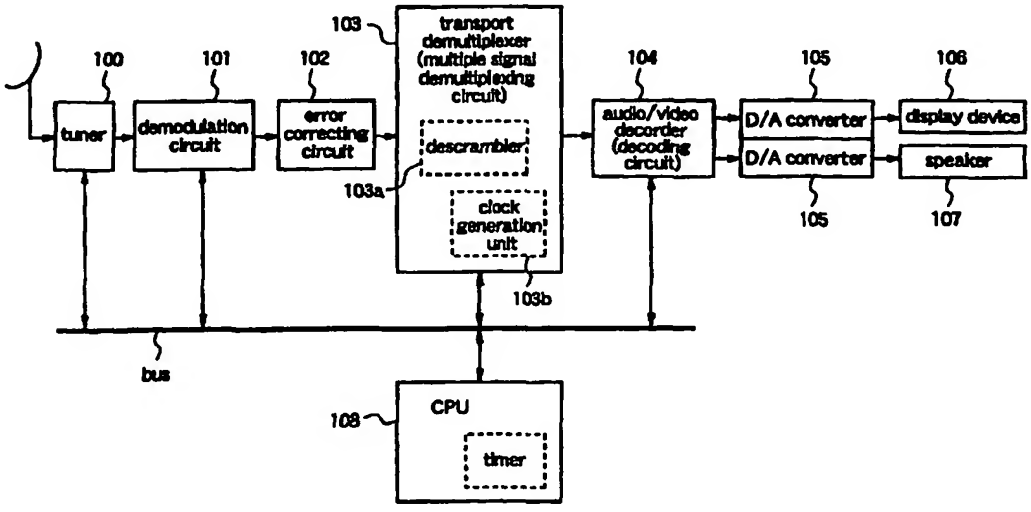
(72) Inventors:
- **TSUJI, Toshiaki**
  Kobe-shi Hyogo 658-0066 (JP)
- **NISHIO, Toshiroh**
  Hirakata-shi Osaka 573-1115 (JP)

(74) Representative:
Eisenführ, Speiser & Partner
Martinistrasse 24
28195 Bremen (DE)

(54) BROADCASTING RECEIVER

(57) When an STB is powered off when it is not used (when it is changed to the sleep mode) for the purpose of power-saving, a difference in a subtracter 11 immediately therebefore is held by a control circuit 12 and an oscillation circuit 15 is controlled on the basis of the difference, thereby performing reserved processing at a correct time even when the STB is in the sleep mode.

Fig.1



EP 1 028 535 A1

Description

Technical Field

[0001] The present invention relates to a broadcasting receiver and, more particularly, to a broadcasting receiver having a power-saving (sleep) mode for reducing power consumption on standby, where precision of an internal timer is improved.

Background Art

[0002] In recent years, plural broadcasting satellites are launched, and thereby digital broadcastings using the satellite waves are started by plural broadcast distributors. In order to receive services of the broadcastings, a set top box (hereinafter, also referred to as STB) should be installed as a receiver, which is to be a decoder for decoding compressed signals of the received broadcasting and converting the same into signals which can be displayed on a display unit such as CRT.

[0003] Fig.5 is a block diagram mainly illustrating a clock generation unit in a STB as the above-described receiver, which is shown in the standards of MPEG, "ISO/IEC 13818-1 generic coding of moving pictures and associated audio: systems, Annex D.0.3 System Time Clock recovery in the decoder". In the figure, reference numeral 10 denotes a capture PCR for capturing a PCR (Program Clock Reference) indicating a broadcasting time for each program, which is included in a transport stream. Numeral 11 denotes a subtracter for generating a difference between an output of an STC counter, which will be described later, and an output of the capture PCR 10. Numeral 13 denotes a low-pass filter for cutting high frequency components more than a predetermined value so as to prevent an oscillation circuit 15, which will be described later, from significantly fluctuating (diverging) when the difference is abruptly changed. Numeral 14 denotes a D/A converter for converting a signal which passed through the filter 13 into an analog signal. Numeral 15 denotes an oscillation circuit, such as a voltage controlled oscillator (VCO), oscillation frequencies of which are controlled by an analog signal (voltage). Numeral 16 denotes an STC (System Time Clock) counter operating with a frequency signal (clock) output from the oscillation circuit 15 and functioning as an internal timer in the system. In addition, around this clock generation unit, circuits such as a tuner for selecting a channel or a decoder for decoding data are placed.

[0004] Using the above-described structure, a predetermined frequency signal is generated on the basis of a PCR indicating a broadcasting time for each program, which is included in the transport stream, and the internal timer in the system is operated. That is, the PCR detected by the capture PCR 10 is converted into an analog signal by the D/A converter 14, after its high frequency components more than the predetermined value are cut off by the filter 13. Then, the oscillation circuit 15 receives the converted analog signal (voltage) as an input and outputs a frequency signal, and the STC counter 16 in the latter stage operates with the frequency signal. Then, a difference between the output of the STC counter 16 and the output of the capture PCR 10 is generated by the subtracter 11. By adjusting a loop from the subtracter 11 to the STC counter 16 so as to have the difference of "0", a clock in synchronization with an input signal can be reproduced.

[0005] Anyhow, in recent years, there are some household electrical appliances in which the power consumption during standby when they are not used is not so smaller than that during operation.

[0006] Also in the STB, as in a television apparatus, it is considered to be preferable that unnecessary elements, such as a tuner or a decoder, should be powered off when they are not used, i.e., they are not in operation. Therefore, some STBs are constructed so as to be in the sleep mode (referred to also as an operation standby state) till a reserved processing start time. However, since reservation processings are performed with respect to playback/recording or the like in the STB, when the power is turned off for a long time, an error occurs in the internal timer and the reserved processing cannot be executed at a correct time.

[0007] The conventional broadcasting receiver is constructed as described above, and it does not have a structure for realizing lower power consumption on standby or, even when it has a structure which can put the STB into the sleep mode for the lower power consumption, it cannot perform the reserved processing at a correct time due to the error in the internal timer.

[0008] The present invention is made to solve the above-described problems and it is an object of the present invention to provide a broadcasting receiver which can perform the reserved processing at a correct time even when the STB is put into the sleep mode.

Disclosure of the Invention

[0009] A broadcasting receiver according to Claim 1 of the present invention, which generates a clock of a predetermined frequency on the basis of a reference signal included in digital data including time-axis information and has an internal timer operating with the clock, comprises: reference signal detection means for detecting the reference signal; clock generation means for generating a clock of a frequency on the basis of the reference signal; counter means for counting the clock; difference generation means for calculating a time difference between output of the counter means and the reference signal; and control means for holding the output of the clock generation means when the receiver is changed to an operation standby state.

[0010] According to Claim 2 of the present invention, in the broadcasting receiver of Claim 1, when the

receiver is in the operation standby state, the reference signal detection means detects the reference signal, the holding operation of the control means is released, and the receiver is put into an operation state for a prescribed time.

[0011] According to Claim 3 of the present invention, in the broadcasting receiver of Claim 1, a transport stream is utilized as the digital data including the time-axis information and a PCR (Program Clock Reference) indicating a broadcasting time for each program is utilized as the reference signal.

[0012] According to Claim 4 of the present invention, in the broadcasting receiver of Claim 1, a transport stream is utilized as the digital data including the time-axis information and a TDT (Time and Data Table) indicating a broadcasting time for each program is utilized as the reference signal.

[0013] As described above, according to the broadcasting receiver of the present invention, when the STB is changed into the sleep mode, a difference is immediately is held by the control circuit and the oscillation circuit is controlled on the basis of the difference. Therefore, even in the sleep mode when the PCR cannot be detected, the great divergence of the oscillation frequencies can be avoided, whereby processings such as reserved processings can be performed on time.

[0014] In addition, the receiver is started at a uniform time interval during the sleep mode, receives the transport stream to detect the reference signal, and thereby occasionally corrects the time. Therefore, the precision of the internal timer can be further improved.

Brief Description of the Drawings

[0015]

Fig.1 is a block diagram illustrating a whole structure of a broadcasting receiver according to a first embodiment of the present invention.

Fig.2 is a block diagram illustrating mainly a clock generation unit in the broadcasting receiver according to the first embodiment.

Fig.3 is a diagram illustrating an example of a transport stream input to the clock generation unit in the broadcasting receiver of the first embodiment.

Fig.4 is a block diagram illustrating mainly a clock generation unit in a broadcasting receiver according to a second embodiment of the present invention.

Fig.5 is a block diagram illustrating mainly a clock generation unit in a prior art broadcasting receiver.

Best Mode for Carrying Out the Invention

[0016] Hereinafter, embodiments of a broadcasting receiver of the present invention will be described with reference to the drawings.

Embodiment 1.

[0017] Fig.1 is a block diagram illustrating a whole structure of an STB as a broadcasting receiver according to a first embodiment of the present invention. In the figure, reference numeral 100 denotes a tuner for receiving a broadcasting signal and selecting a desired channel. Numeral 101 denotes a demodulation circuit for demodulating a digital signal sequence of signals in the channel selected by the tuner. Numeral 102 denotes an error correcting circuit for performing error correction for the demodulated digital signal sequence. Numeral 103 denotes a transport demultiplexer (multiplexed signal demultiplexing circuit) for selecting one transport stream from plural transport streams included in the digital signal sequence and further extracting a digital signal sequence of only a desired program. Numeral 104 denotes an audio/video decoder (decoding circuit) for decoding the digital signal sequence extracted from the transport demultiplexer 103 into decompressed digital signals. Numeral 105 denotes a D/A converter for converting audio/video in digital form into audio/video in analog form. Numeral 106 denotes a display device, such as a CRT. Numeral 107 denotes a speaker. Numeral 108 denotes a CPU for controlling operations of the respective elements via a bus. In addition, the transport demultiplexer 103 includes a descrambler circuit 103a for descrambling a scrambled signal of fee-charged broadcasting or the like, and a clock generation unit 103b.

[0018] Fig.2 is a diagram illustrating a structure of a clock generation unit in the broadcasting receiver of the first embodiment. In the figure, reference numeral 10 denotes a capture PCR for capturing a PCR (Program Clock Reference) indicating a broadcasting time for each program, which is included in the transport stream. Numeral 11 denotes a subtracter for generating a difference between an output of an STC counter, which will be described later, and an output of the capture PCR 10. Numeral 12 denotes a control circuit operating upon receipt of a power management control signal which is used when the apparatus is changed into the sleep mode and holding the difference of the subtracter 11. This control circuit is realized, for example, by a well-known latch circuit or a flip-flop (FF) with Load/Hold. Further, numeral 13 denotes a low-pass filter for cutting high frequency components more than a predetermined value so as to prevent an oscillation circuit 15, which will be described later, from significantly fluctuating (diverging) when the difference is abruptly changed. Numeral 14 denotes a D/A converter for converting a signal which passed the filter 13 into an analog signal. Numeral 15 denotes an oscillation circuit, such as a voltage controlled oscillator (VCO), oscillation frequencies of which are controlled by an analog signal (voltage). Numeral 16 denotes an STC (System Time Clock) counter operating with a frequency signal (clock) output from the osciliation circuit 15 and functioning as an

internal timer in the system.

[0019] Next, an operation of the STB when the power is turned on will be described. The capture PCR 10 captures a PCR included in a transport stream and outputs the same. Fig.3 shows an example of the transport stream, which comprises a header at the head, followed by an adaptation field, video data (Pay Load), ... A PCR is data existing within the adaptation field having control information described thereon and, practically, data transmitted at intervals of 100 msec. or shorter. At this time, since the power management control signal (PMC) is not input, the control circuit 12 outputs the data which passed through the subtracter 11 as it is to the filter 13 in the next stage. High frequency components of signals more than the predetermined value are removed from the data by the filter 13 and signals are converted into analog signals by the D/A converter 14 in the next stage. Then, the oscillation circuit 15 generates a clock of a frequency corresponding to the input, according to the converted analog signal. The STC counter 16 operates with this clock, for example a 27-MHz clock, and performs a timer operation on the clock as the reference of the system. Then, in the subtracter 11, a difference between the output of the STC counter 16 and an input PCR signal is generated. When the output of the oscillation circuit 15 has a frequency coinciding with the transmitted PCR, the difference is zero and a stable clock is reproduced.

[0020] In the above-described state, when a reservation processing or the like is performed and the system is not required to be started till the reserved processing start, the system is put into the sleep mode and the operations of most parts of the system are stopped by the power management control signal. Then, the capture PCR 10 cannot detect the PCR. At the same time, the control circuit 12 starts its operation and holds the difference of the subtracter 11 just before the powering off.

[0021] Thereafter, the output of the oscillation circuit 15 is controlled on the basis of the difference held by the control circuit 12.

[0022] In this way, also after the system is changed into the sleep mode, a relatively stable clock can be reproduced. However, due to a transmission jitter (fluctuation) of the PCR itself, a divergence in time has already arisen sometimes when the difference is held at the changing to the sleep mode.

[0023] In this embodiment, the system is automatically started once a prescribed time after the sleep mode, thereby receiving a transport stream to correct the time. Assume that the transmission jitter of PCR is ±100 ppm, a maximum of 100-ppm divergence is generated. In this case, when a 27-MHz clock is to be reproduced, the clock is changed to 27.0027MHz. When the system is put into the sleep mode for 30 minutes. with this error, a divergence of 0.18 seconds. is generated. Accordingly, the system is started every three hours to receive the transport stream, whereby the error is reduced to within 1 second. Therefore, there is no problem with the precision of the internal timer of the system for practical use.

[0024] While the power is consumed at this time, for example, the STB consumes about 10W/H of power in the normal operation and about 0.5W/H in the sleep mode. Therefore, even when the system is operated for 5 minutes, in the sleep mode, the system consumes only about 0.7-0.8W/H of power and the increase in the power consumption due to that operation is almost insignificant.

[0025] As described above, according to this embodiment, when the STB is changed into the sleep mode, the control circuit 12 holds the difference of the subtracter 11 immediately therebefore and the oscillation circuit 15 is controlled on the basis of the difference. Therefore, also in the sleep mode when the PCR cannot be detected, the great divergence of the oscillation frequencies can be avoided, resulting in an improved precision in the internal timer. Consequently, processings such as the reserved processing can be performed on time.

[0026] In addition, the system is started at a uniform time interval during the sleep mode to receive the transport stream, detect the PCR, and occasionally correct the time, whereby the precision in the internal timer is further improved.

Embodiment 2.

[0027] Hereinafter, a broadcasting receiver according to a second embodiment of the present invention will be described with reference to the drawings. While in the first embodiment the clock is reproduced by detecting the PCR, the second embodiment is different from the first embodiment in that the clock is reproduced by detecting a TDT (Time and Data Table) included in the transport stream.

[0028] As shown in fig.4, the broadcasting receiver of the second embodiment includes a capture TDT 17 in place of the capture PCR and other construction is the same as that in the first embodiment. The TDT in this case is transmitted every two seconds. By detecting this TDT, the present invention can be similarly applied to a construction where the clock is reproduced on the basis of the TDT. According to this construction, while the precision is inferior to that in the first embodiment, the degree of inferiority is of negligible level for the practical use.

[0029] In the respective embodiments, the control circuit 12 is placed just behind the subtracter 11, because noises due to disturbance of signals can be reduced more effectively than in a case where the control circuit is placed in the latter stage of the filter. Therefore, in a case where superimposition of noise does not matter, the control circuit can be provided in other positions, such as just behind the filter 13 or the D/A converter, or just behind the capture PCR 10 and the STC

counter 16.

Industrial Availability

[0030] The present invention relates to a broadcasting receiver and particularly improves precision in an internal timer of a broadcasting receiver having a power-saving (sleep) mode for reducing power consumption on standby, thereby enabling to perform a reserved processing, such as a reserved recording, with certainty.

Claims

1. A broadcasting receiver which generates a clock of a predetermined frequency on the basis of a reference signal included in digital data including time-axis information, and has an internal timer operating with the clock, comprising:

   reference signal detection means for detecting the reference signal;
   clock generation means for generating a clock of a frequency on the basis of the reference signal;
   counter means for counting the clock;
   difference generation means for calculating a time difference between output of the counter means and the reference signal; and
   control means for holding the output of the clock generation means when the receiver is changed to an operation standby state.

2. The broadcasting receiver of Claim 1 wherein

   when the receiver is in the operation standby state, the reference signal detection means detects the reference signal, the holding operation of the control means is released, whereby the receiver is put into an operation state for a prescribed time.

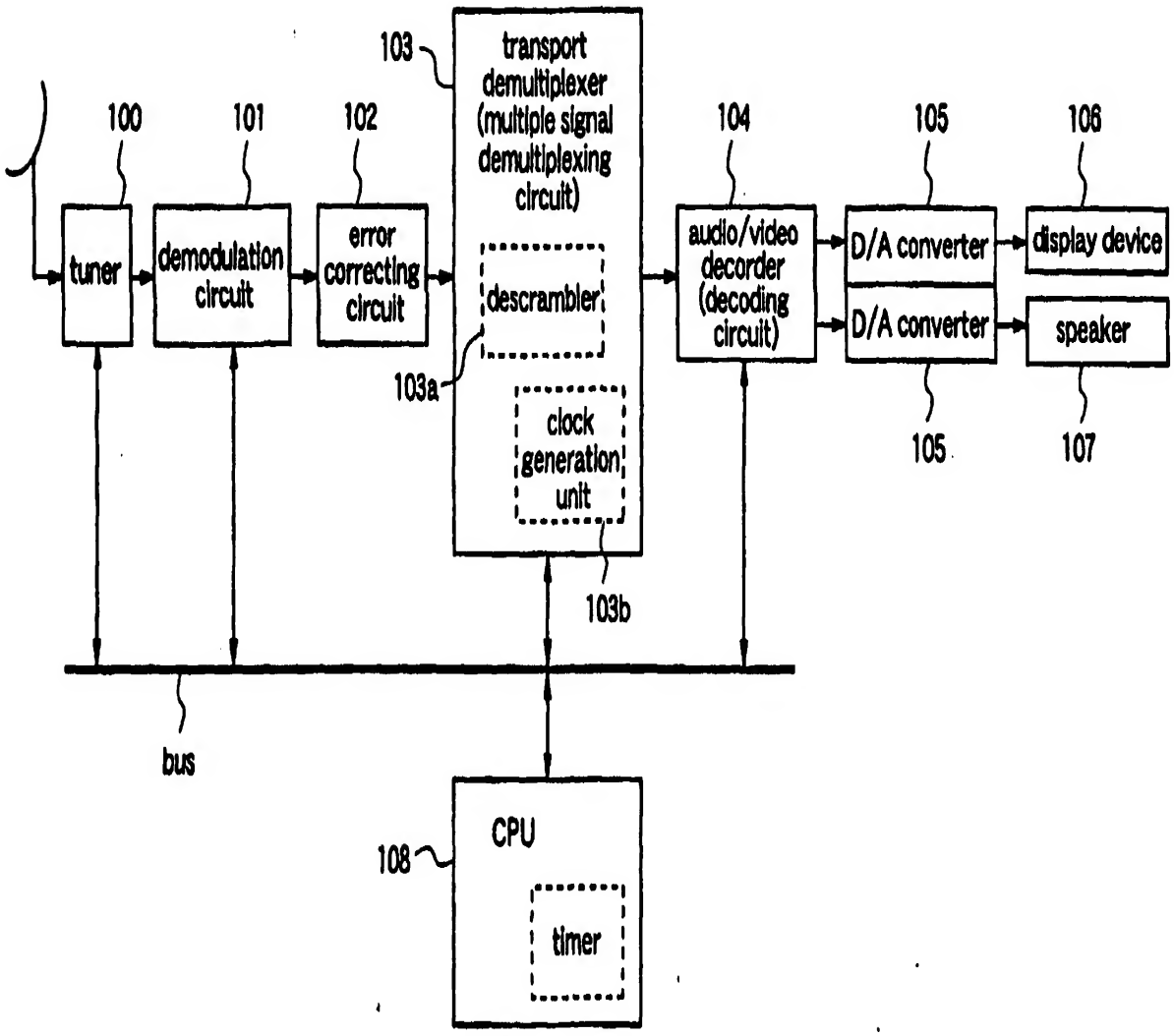
3. The broadcasting receiver of Claim 1 wherein

   a transport stream is utilized as the digital data including the time-axis information and a PCR (Program Clock Reference) indicating a broadcasting time for each program is utilized as the reference signal.

4. The broadcasting receiver of Claim 1 wherein

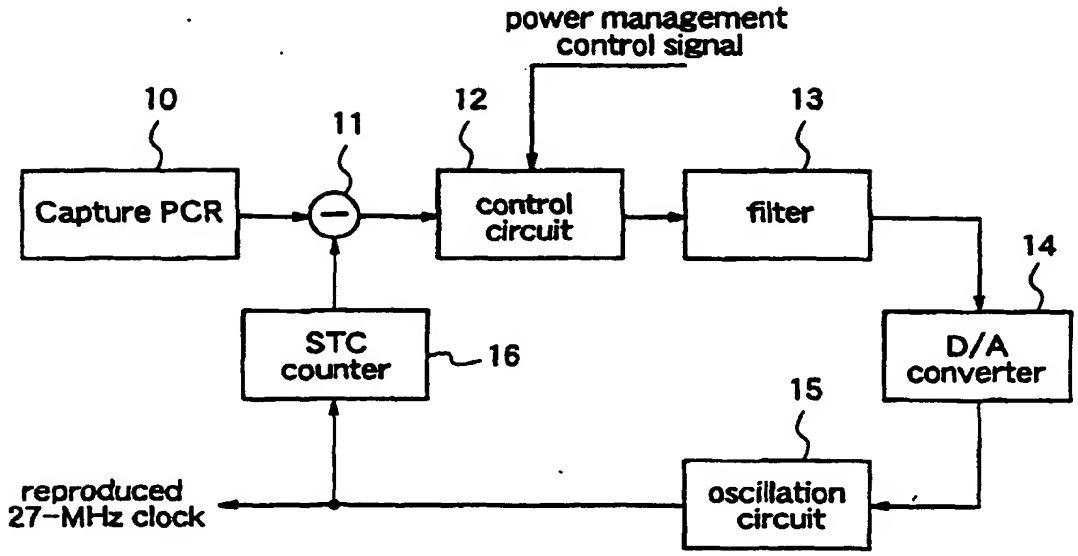
   a transport stream is utilized as the digital data including the time-axis information and a TDT (Time and Data Table) indicating a broadcasting time for each program is utilized as the reference signal.

Fig.1



EP 1 028 535 A1

Fig.2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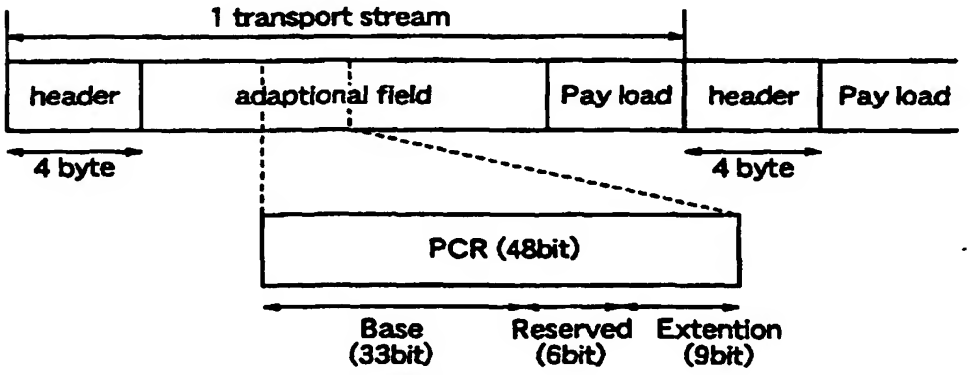
control signal
10
11
12
13
Capture PCR
control
circuit
filter
14
STC
counter
16
D/A
converter
15
reproduced
27-MHz clock
oscillation
circuit

Fig.3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header
adaptional field
Pay load
header
Pay load
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4 byte
PCR (48bit)
Base
(33bit)
Reserved
(6bit)
Extention
(9bit)

Fig.4

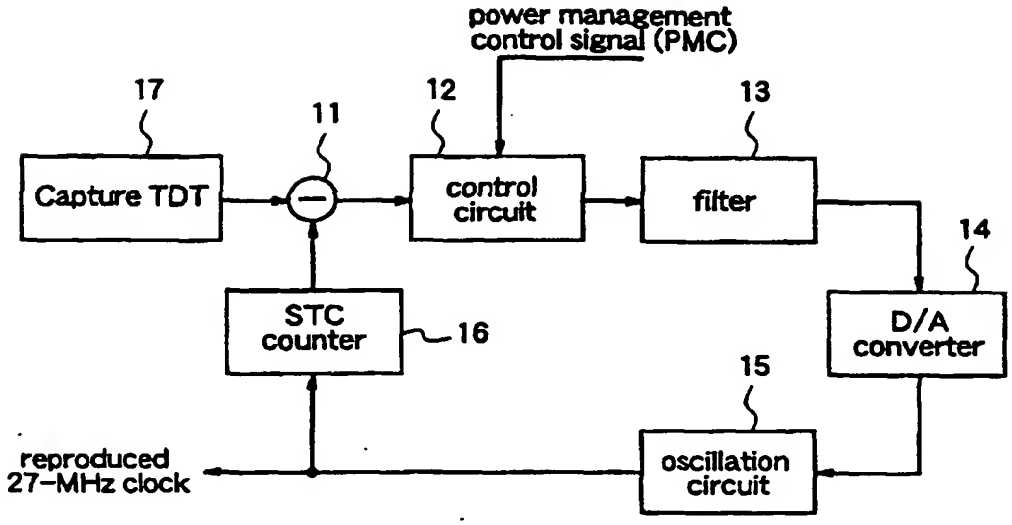
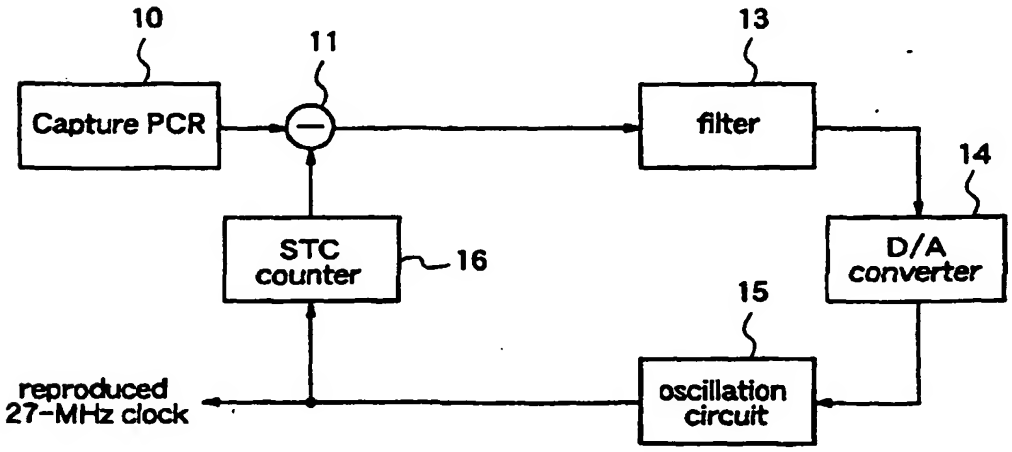

power management
control signal (PMC)
17
11
12
13
Capture TDT
control
circuit
filter
14
STC
counter
16
D/A
converter
15
reproduced
27-MHz clock
oscillation
circuit

Fig.5


10
11
13
Capture PCR
filter
14
STC
counter
16
D/A
converter
15
reproduced
27-MHz clock
oscillation
circuit

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP99/03068

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[6] H04B1/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[6] H04B1/16, G06F1/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-1998
Kokai Jitsuyo Shinan Koho 1971-1996 Jitsuyo Shinan Toroku Koho 1996-1998

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 8-161076, A (Matsushita Electric Industrial Co., Ltd.), 21 June, 1996 (21. 06. 96) (Family: none)	1-4
A	JP, 6-180617, A (Izuru Haruhara), 28 June, 1994 (28. 06. 94) (Family: none)	1-4
A	JP, 57-130133, A (Tokyo Shibaura Electric Co., Ltd.), 12 August, 1982 (12. 08. 82) (Family: none)	1-4

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 August, 1999 (27. 08. 99)	14 September, 1999 (14. 09. 99)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

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